Charles

Telecommunications Group

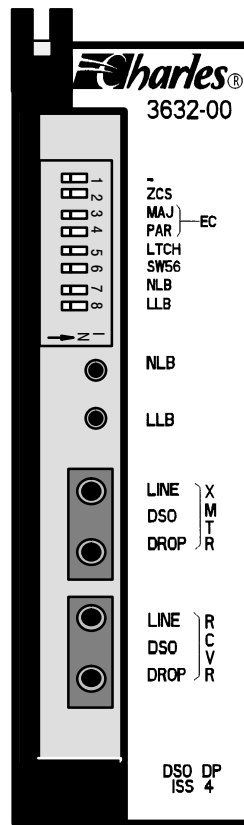# 3632–00 Digital Signal Level Zero Data Port (DS–0 DP) Channel Unit

Figure 1. 3632−00 DS−0 DP Channel Unit

1. GENERAL

1.1 Document Purpose

This document provides information for the Charles Industries 3632–00 DS–0 DP Channel Unit, shown in Figure 1.

1.2 Document Status

This document is reprinted to add the new Issue 4 features: two-channel parity error correction, latching loopback detection, switched 56 kilobit signaling decoding, and manual network or local loopback capability.

1.3 Equipment Function

The 3632–00 is a synchronous data channel unit that provides an interface between a DS–0 level intra-office data signal and one channel time slot of a channel bank.

1.4 Equipment Location/Mounting

The 3632–00 DS–0 DP installs in one channel slot of a 360/363 D4 Channel Bank and provides the associated digital carrier facility with a 4-wire DS–0 level data port. The DS–0 level signal is a 64KB/s synchronous data signal having a bipolar NRZ format. Two types of DS–0 level signals can be passed by the 3632–00: DS–0A and DS–0B. The DS–0A signal contains either redundant information derived by successively repeating each byte of a single non-multiplexed subrate data channel or data from a single 56KB/s baseband data channel. The DS–0B signal contains no redundant information and is derived from a number of individual subrate data channels that have been multiplexed into a common channel.

Each digroup of the 360/363 D4 PCM Channel Bank can be equipped with up to 24 3632–00 DS–0 DP channel units, provided that parity channel error correction is not required. Additionally, use of the 3632–00 DS–0 DP requires that the digroup common equipment contain an LIU–3E module. The LIU–3E provides DDS-compatible BIT and BYTE clock signals for synchronizing the 3632–00. The LIU–3E allows both DDS-compatible data and voice channel units in the same digroup.

1.5 Equipment Features

Features of the 3632–00 include the following:

- Bipolar non-return-to-zero (NRZ) signal format at DS–0 interface

- Selectable zero code suppression circuit

- Selectable 3 out of 5 majority logic error correction for 2.4, 4.8 and 9.6 KB data rates (DS0A).

- Data rate of 64KB/s at DS–0 level

- Bidirectional access to DS–0 via front panel bantam jacks

- Meets Bell Communications Specification TA–TSY–000077

- Switched 56 KB

- Latching loopback (network and local)

- Tandem latching loopback capability

- Manual network and local loopbacks

- Two channel parity error correction for 56 KB and 64 KB data rates

2. INSPECTION

2.1 Inspect for Damages

Inspect the equipment thoroughly upon delivery. If the equipment has been damaged in transit, immediately report the extent of damage to the transportation company.

2.2 Equipment Identification

Charles Industries' equipment is identified by a model and issue number imprinted on the front panel or located elsewhere on the equipment. Each time a major engineering design change is made on the equipment, the issue number is advanced by 1 and imprinted on subsequent units manufactured. Therefore, be sure to include both the model number and its issue number when making inquiries about the equipment.

2.3 Static Concerns

Each module is shipped in static-protective packaging to prevent electrostatic charges from damaging static-sensitive devices. Use approved static-preventive measures, such as static-conductive wrist straps and a static-dissipative mat, when handling modules outside of their protective packaging. A module intended for future use should be tested as soon as possible and returned to its original protective packaging for storage.

STATIC-SENSITIVE

This equipment contains static-sensitive electronic devices. To prevent electrostatic charges from damaging static-sensitive units:

- **Use approved static preventive measures (such as a static-conductive wrist strap and a static-dissipative mat) at all times whenever touching units outside of their original, shipped static-protective packaging.**

- **Do not ship or store units near strong electrostatic, electromagnetic, or magnetic fields.**

- **Use static-protective packaging for shipping or storage.**

3. APPLICATION GUIDELINES

3.1 Intermediate Office Applications

The 3632−00 DS−0 DP can tandem a DS−0A or DS−0B level signal through consecutive digital carrier facilities. See Figure 2. In this application, each of the 360/363 D4 digroups at the tandem office is provided with a 3632−00 DS−0 DP. The data ports are then connected via intra-office wiring to complete the data path between the digital carrier terminals. In order to keep synchronization, the composite clock must be connected between channel banks.

3.2 End Office Applications

The 3632−00 DS−0 DP can also be used at an end office where an integral subrate multiplexer (ISMX) is used to combine a number of subrate data channels into a single digital carrier channel. See Figure 3. The 3632−00 interfaces the DS−0B level port on the line side of the ISMX with the 1.544MB/s T1 bit stream of the carrier facility.
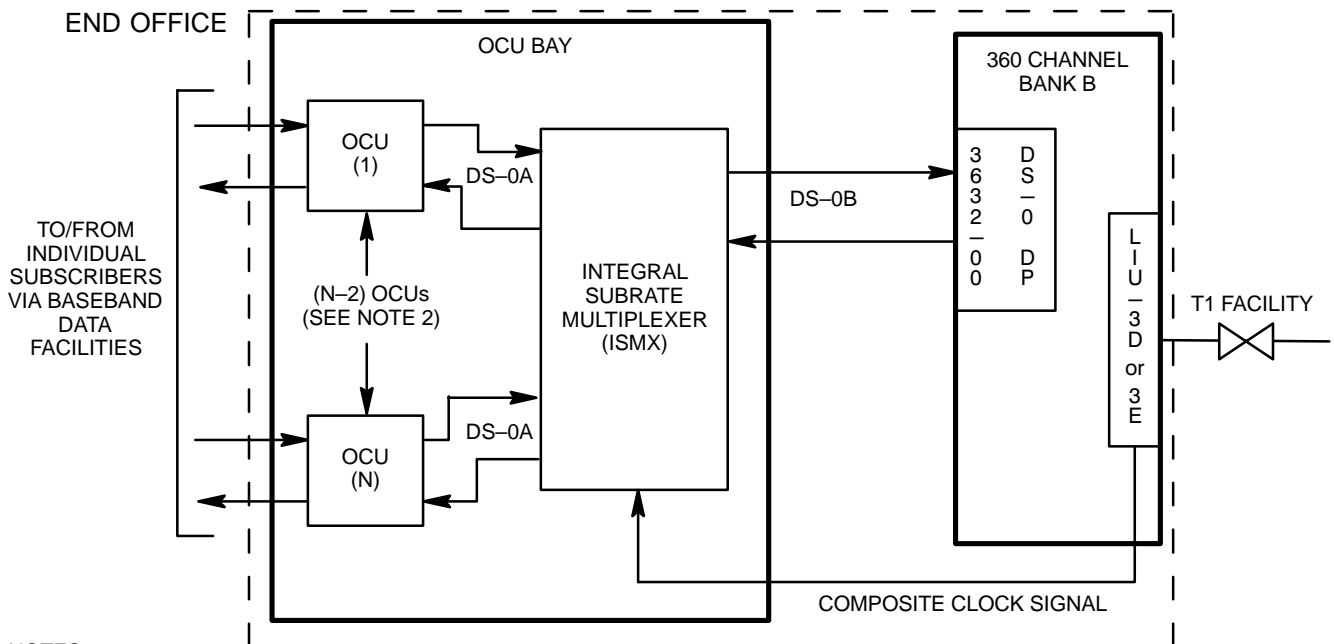
All cross-connects between digital carrier facilities are made at the DS−0A/B level. A typical office, equipped with 3632−00 DS−0 DPs for implementing DS−0A/B cross-connects, is shown in Figure 2. Refer to the notes for option conditioning requirements and supplementary information. The manner in which the channel banks are synchronized with the data network is subject to variation and depends upon network configuration and the location of the subject intermediate office relative to the remainder of the network. For information on synchronizing schemes, refer to the Charles 360 and 363 D4 Digital Carrier Terminal System Overview in Section 360−000−100.

Figure 2. 3632–00 DS–0 DP Applied in Tandem-Connecting Digital Carrier Facilities
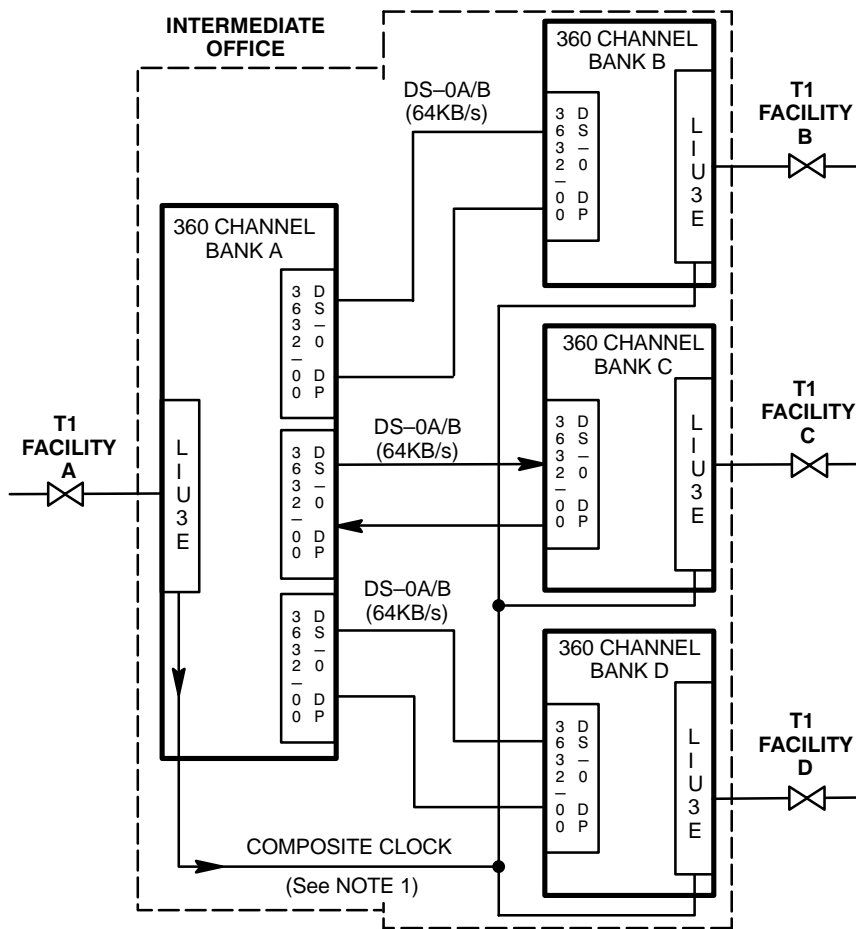
NOTES

1. Channel Bank A through D must be synchronized to the data network. Bank synchronization is provided by options on the LIU–3E.

2. The DS–0 DPs may be cross-connected to any channel slot, due to byte synchronization of the channel banks.

3. If no error correction is required, set both error correction options to OUT. For error correction at data content of 2.4 to 9.6 K, set the MAJ (majority logic) switch to IN. For error correction of all other data content applications, set the PAR (parity channel) error correction switch to IN.

NOTES

1. The 360 Channel Bank must be synchronized to the data network. Bank synchronization is provided by options on the LIU–3E.

2. N, the total number of OCUs that can be provided, depends upon the baseband data rate;
N = 20 for a 2.4KB/s data rate, N = 10 for a 4.8KB/s data rate, N = 5 for a 9.6KB/s data rate, and N=2 for a 19.2 KB/s data rate.

Figure 3. 3632–00 DS–0 DP Applied in Conjunction with an ISMX

3.3   Multiplexing Common Data Channel

When an end office serves a number of subscriber loops at baseband subrates of 9.6KB/s or below, groups of subscriber channels having a common data rate and destination can be multiplexed onto the same digital carrier channel. One arrangement for concentrating subrate data channels uses an integral subrate multiplexer (ISMX), as illustrated in Figure 3. The line side of the ISMX carrying the combined information is at the DS–0B level; hence, a 3632–00 DS–0 DP is required for interfacing with the 360 Channel Bank. When an ISMX is used, the DSX–0B link contains no redundant information, and the majority logic error corrector within the 3632–00 must be disabled. If error correction is required, use parity channel error correction. The use of error correction depends only upon the error rate objectives of the data channel user.

3.4   Synchronization

In Figure 3, the ISMX, as well as the 360 channel bank, must be synchronized with the data network. In an end office, the 360 channel bank is synchronized with the incoming T1 bit stream via option conditioning within the LIU–3E. In turn, the LIU–3E provides a composite clock output signal to synchronize the ISMX. Additional option conditioning information is provided in the notes in Figure 3.

3.5   Voice Channel Link Applications

The 3632–00 can link a voice channel through tandem-connected carrier facilities. However, signaling information on the A and B signaling highways associated with the voice channel cannot be carried since these paths do not appear in the DS–0 level signal. If signaling is required, it can be provided within the voice channel by using 2600Hz SF signaling techniques.

3.6   64KB/s Clear Channel Applications

The 3632–00 can be used for data applications that require the transmission of a 64KB/s clear channel. When this is necessary, the 3603–02/32 LIU–3E and the 3608–02/32 DIU must be used as common equipment in the 360/363 Channel Bank. This set of common equipment provides the B8ZS feature and the extended super frame (ESF) format. B8ZS must be enabled at both ends of the T1 line. The B8ZS feature prevents strings of zeros from being transmitted on the T1 line. Zero strings are transmitted as formatted words with bipolar violations that are then decoded at the distant terminal.

4.   CIRCUIT DESCRIPTION

Refer to Figure 4 (3632–00 DS–0 DP Block Diagram) and to the application drawings (Figure 2 and Figure 3) while reading the following description.

4.1   Transmit Operation (DS–0 to T1 Direction)

The DS–0 level data signal from the intra-office cross-connect path enters the 3632–00 on pins 50 (tip) and 48 (ring) and is passed through the RCVR DROP and XMTR LINE jacks to the primary of transformer T1. The jacks eliminate the need for a cross-connect patch panel and provide access points looking toward both directions. They are used in conjunction with similar jacks in the drop side of the receive path for connecting KS–20909/KS–20908 test sets (or equivalent) or for manually initiating loopback via a patch cord. Transformer T1 provides a balanced, DC-isolated path to the bipolar receiver and matches its input to the 135-ohm impedance of the DS–0 path.

The buffer register provides elastic storage which compensates for the variable timing relationship between the channel bank timing and the DDS-compatible bit and byte clock. The 64KB to T1 buffer register is synchronized to the data network via signals from the DDS bit clock and DDS byte clock leads of the terminal's LIU–3E module.

The bipolar receiver converts the data signal to a unipolar format. This signal is then connected to a custom field programmable gate array (FPGA) IC that performs both transmit and receive selected data manipulation. Depending on which option is selected via the front panel switches, different portions of the internal FPGA circuit will be enabled.

In the first portion of the transmit data processing of this FPGA IC, latching loopback code may be detected if enabled (via the front panel LTCH switch). This will cause a loopback of the data towards the local DS–0 loop. If the front panel local loopback (LLB) switch is enabled, it forces a loopback of data towards the local DS–0 loop also. The front panel LLB LED will light for both of these conditions and "3C HEX" will be transmitted to the T1 network.

If the front panel zero code (ZC) switch is turned on, any data byte to be transmitted to the T1/DS1 Network which has all eight of its bits low or at a zero state will be converted to unassigned multiplexer code (00011000).
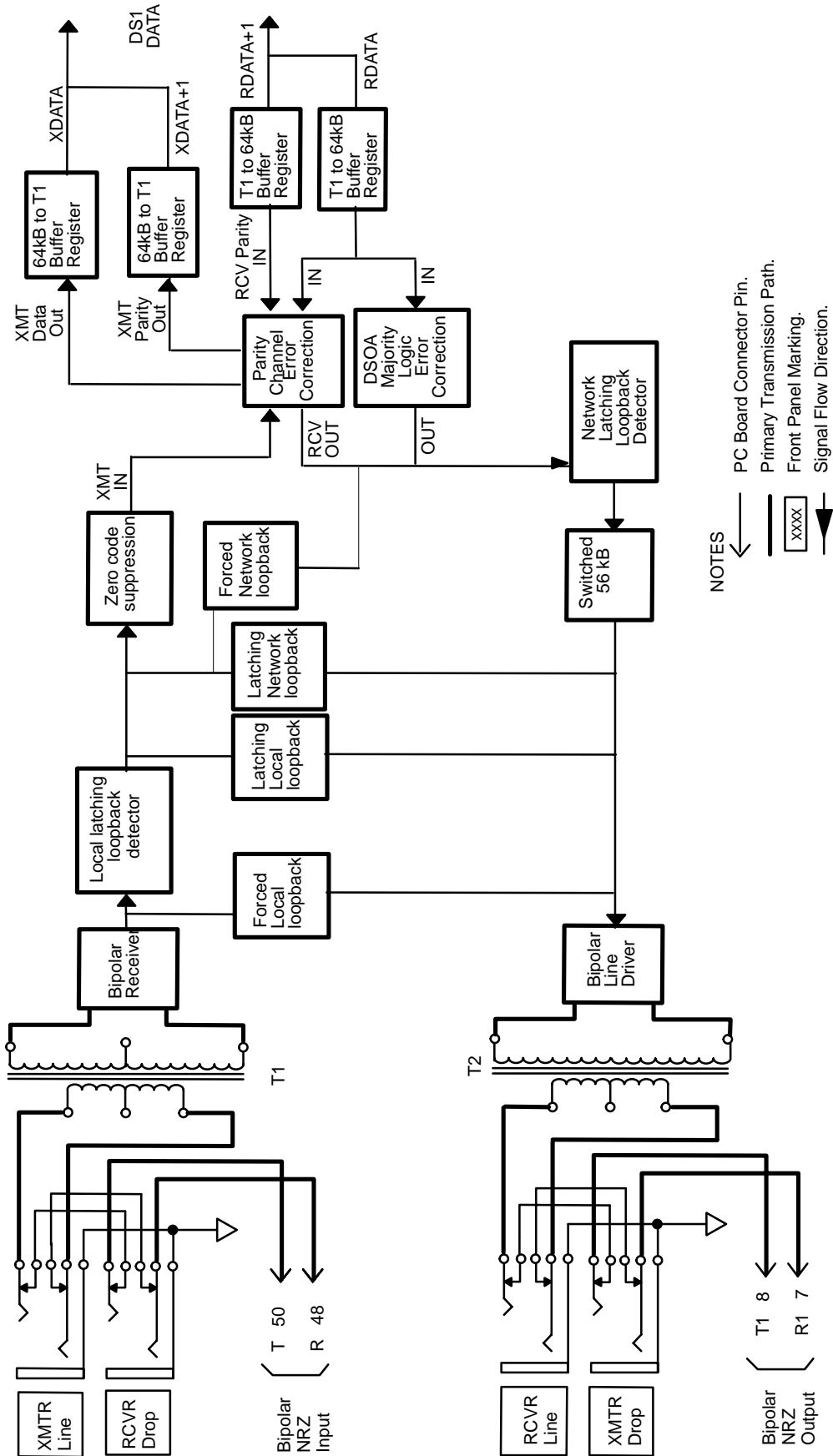
Figure 4. 3632−00 DS−0 DP Channel Unit Block Diagram

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When 56KB/s or multiplexed subrate data is passed on the DS−0 channel, parity channel error correction can be provided (if required). When parity channel error correction is used, compatible correction must also be used in the corresponding channel unit at the opposite end of the carrier facility. When parity channel error correction of this type is chosen, the 8-bit data byte is encoded with an algebraic coding algorithm to derive a second 8-bit byte (called a parity byte) that is used for parity channel error correction. The code used is a modified BCH (Base-Chaudhuri-Hocquenghem) code. When received and decoded, the BCH code is structured to correct any single or double bit error in the 16 bits, and about 1/3 of the cases with three bits in error can be corrected. During this operation, the majority logic error correction is inhibited. When parity channel error correction (PAR EC) is turned on via the front panel switch, an eight bit parity byte will be added to the transmitted data information for a total of 16 bits. The card will use the time slot associated with the slot the card is plugged into and the next time slot after it for input and output. If error correction of this type is not used, just the 8-bit byte of data enters the 64KB to T1 buffer register to be transmitted toward the T1/DS1 Network.

4.2   Receive Operation (T1 to DS−0 Direction)

The incoming 1.544 MB/s bit stream containing information pertaining to all 24 channels is routed from the common RCV DATA bus to the DS−0 DP. Upon entering the card, the data is routed to the T1 TO 64KB BUFFER REGISTER portion of the FPGA, which provides elastic storage to compensate for the variable timing relationship that exists between the channel bank timing and the DDS-compatible bit and byte clocks. This buffer register admits incoming information only during the time that corresponds with the channel position occupied by the DS−0 DP within the 24-channel frame of the digroup. During the channel time interval, the incoming 8-bit byte is received serially into the elastic storage within the buffer register Subsequently, it is transferred out of the buffer register at the 64KB/s DS−0 rate under the control of signals received on the DDS BIT CLOCK and DDS BYTE CLOCK buses from the terminal's LIU−3E module.

If parity channel error correction was enabled for transmission of data or is being performed at the far end T1 connected system, then the receive data, which will be two 8-bit bytes, will be decoded to check for parity matching. Correction for up to two bits in error will be performed via this circuit portion of the FPGA.

If the data signal being passed through the DS−0 channel contains redundant information (i.e., non-multiplexed subrate data (DS0A)), error correction for subrates can be applied at this point. In this case, error correction is applied by turning on the MAJ EC front panel switch. This causes the output of the buffer register to be routed through the majority logic error correction portion of the FPGA. This error correction monitors for inconsistencies among five bytes of redundant data and corrects each bit individually to the majority condition.

If latching loopback (LTCH) was enabled via the front panel option switch, when network loopback codes are detected the received network data will be transmitted back to the T1/DS1 network. The front panel NLB LED will light and "idle code" (FE HEX) will be transmitted to the customer DS0 drop.

If the front panel network loopback (NLB) switch is turned on, received data from the DS1/T1 network for this time slot will be looped back towards T1/DS1 network. The front panel NLB LED will light.

If the switched 56KB (SW56) front panel option switch is turned on, the DS0−DP can be used by the local exchange carrier (LEC) to offer dedicated digital access to interexchange carrier (ICC) switched digital data services. In switched 56 applications, the DS0−DP stuffs the received A signaling highway bit into every transmitted DS−0 byte towards the loop.

In the event of a failure of the incoming T1 bit stream framing signal, the terminal's common equipment sends a carrier group alarm immediate (CGAI) signal to this unit. This signal activates the multiplexer-out-of-sync code generator in this unit whose output overrides the data inputted to the bipolar line driver. Thus, the alarm condition is transmitted down the DS−0 cross-connect line using the MUX-out-of-sync code (00011010 (hex 1,A)).

WARNING

When the data port is configured for no error correction or majority logic error correction, a single time slot is used and the unit may be located in any channel slot. With parity channel error correction selected, the data port generates parity for each data byte and occupies two time slots. Therefore, this unit cannot be located in time slot 24 when this function of error correction is enabled.

5.   MOUNTING

The 3632−00 mounts in one channel unit slot of a 360/363 D4 Channel Bank. The 3632−00 is equipped with an insert/eject lever in the form of a top-hinged front panel. The insert/eject lever ensures positive connection of a channel unit's card-edge connector to the backplane connector when the unit is installed and provides easy removal of the unit.

CAUTION

Installation and removal of modules should be done with care. Do not force a module into place. If excessive resistance is encountered while installing a module, remove the module and check the card guides and connector to verify proper alignment and the absence of foreign material.

6. INSTALLER CONNECTIONS

6.1 Connectorized 360/363 D4 Channel Banks

On connectorized 360/363 D4 Channel Banks (360–10, –11. etc.) connections are made via 25-pair female connectors (CINCH 222–22–50–023 or equivalent) to the appropriate 25–pair male connectors of the 360/363 D4 Channel Bank. Refer to Section 360–000–200 for the wiring diagrams of the female connectors with respect to the 360/363 D4 Channel Bank being used. The only installer connections necessary for this channel unit are the T and R and T1 and R1 leads

6.2 Non-Connectorized 360/363 D4 Channel Bank

When installing a 3632–00 channel unit into a non-connectorized 360–00/363–00 D4 Channel Bank, make the required connections as shown in Table 1.

Table 1. 3632–00 Installer Connections

Lead Designation		PIN
T (input pair)	DS–0 Bipolar	50
R (Input pair)	DS–0 Bipolar	48
T1 (output pair)	DS–0 Bipolar	8
R1 (output pair)	DS–0 Bipolar	7

Installer connections are made to the channel unit by wire-wrapping leads onto the associated 50–pin connectors on the backplane assembly of the 360–00 or 363–00 D4 Channel Bank.

7. OPTIONS

The 3632–00 DS–0 DP options include implementation of error correction, latching and manual loopback, 56 kB switching and selection of zero code suppression or clear channel operation. See Table 2. Error correction only affects those errors incurred on the T1 carrier facility, and does not affect those errors incurred on the drop sides of either carrier terminal. The decision to use error correction depends upon the maximum error rate objective of the data channel user. Both ends of the carrier facility must be treated in a similar manner when using parity channel error correction.

7.1 Error Correction (EC)

Two types of error correction are available: majority-logic error correction, and parity-channel error correction. The decision to use one type of error correction over the other depends upon the presence of redundant information in the data signal. When the DS–0 cross-connect path carries the non-multiplexed data signal of a single subscriber originating as a subrate data signal of 9.6KB/s or below, use majority logic error corrections by setting the EC MAJ switch to the IN.

When the DS–0 cross-connect path carries the multiplexed data signals of a number of subrate subscribers or the data of a single subscriber originating at rates from 19.2 to 64 KB, use parity-channel error correction. Option the opposite end of the carrier facility identically.

7.2 Zero Code Suppression (ZCS)

Set ZCS IN to enable the zero code suppression circuit for all applications except clear channel applications. Set ZCS OUT to disable zero code suppression for clear channel applications.

7.3   Latching Loopback (LTCH)

Use this option to allow the DS−0 data port to recognize and respond to latching loopback codes. Enable this option by setting the LTCH switch IN. For most applications, this option should be enabled.

If a special application requires that the DS0 DP not recognize latching looping codes, set the LTCH switch OUT.
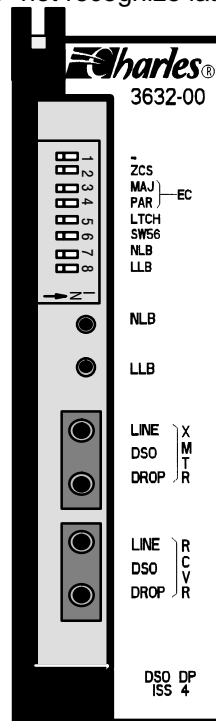

Figure 5.   3632−00 DS−0 DP Channel Unit Option Locations

Table 2.   3632−00 DS−0 DP Channel Unit Optioning Summary

Option	Position	Function
–	N/A	Not used (leave in the OUT position).
ZCS	IN	Enables the zero code suppression circuit. This circuit converts all bytes received having all-zeros for bits one through eight, to the unassigned multiplexer code (00011000) which is transmitted toward the T1 facility. Use this position if data content is 56k or lower.
	OUT	Disables the zero code suppression circuit and provides a 64KB clear channel.
MAJ EC	IN	Activates majority-logic error correction (for DS−0A rates of 2.4, 4.8 and 9.6 kbps). Use if data content is 9.6 k or lower.
	OUT	Deactivates the internal majority-logic error correction.
PAR EC	IN	Enables parity channel error correction; disables majority logic error correction.
	OUT	Disables parity channel error correction.
LTCH	IN	Enables network and local latching loopback code detectors. If latching loopback codes are detected, data is returned to either the T1/DS1 network or the local customer loop, and the respective NLB or LLB LED is lit. Use this position for normal applications.
	OUT	Disables network and local latching loopback.
SW56	IN	Enables switched 56kB operation for SW56 kB applications.
	OUT	Disables switched 56kB operation for all other applications.

Option	Position	Function
NLB	IN	Enables a manual T1/DS1 network loopback (NLB/DSL1P) which causes the receive T1/DS1 network data (RDATA) to be transferred back to the T1/DS1 network (XDATA) and lights the NLB LED.
	OUT	Disables the manual T1/DS1 network loopback for normal channel operation.
LLB	IN	Enables a manual local loopback which causes the customer data that would have been transmitted to the T1/DS1 network to be returned to the customer, and lights the LLB LED.
	OUT	Disables manual local loopback for normal channel operation.

7.4   Switch 56 kB (SW56)

Use this switch to set switch 56 kB operation. In 56 kB operation, signaling highways are used by the subscriber end data ports to indicate the line condition to the service provider. If this type of application goes through tandem DS0 data ports, the signaling highways can be lost. This is because the DS0 arriving on one DS0 DP in a signaling highway frame may not end up on a signaling highway frame on the cross-connect DS0 data port. When the SW56 switch is enabled (set IN), the DS0 data port will look at the incoming signaling highway and change bit 8 of all DS0 bytes to the same value as the signaling highway bit. The cross-connected DS0 data port will have the highway bit on all DS0 bytes so it will also appear on the signaling highway frame going out on the T1 of the cross-connected DS0 DP bank. For all other applications, this option should be disabled (OUT).

7.5   Network Loopback (NLB)

Use this switch to initiate loopback on the T1 side of the data port. This lights the front panel NLB LED.

Set the switch to IN to initiate loopback. Once testing is done and for normal operation, set the switch to OUT to disable loopback.

7.6   Local Loopback (LLB)

Use this switch to initiate loopback on the local equipment side of the data port. This will cause the front panel LLB LED to light.

Set the switch to IN to initiate loopback. Once testing is done and for normal operation, set the switch to OUT to disable loopback.

8.   TESTING

After completing installation, use the following steps to test the unit:

Step	Action
1.	Connect a KS–20909 (or equivalent) Data Test Set (Transmitter) to the XMTR LINE jack, and connect a KS–20908 (or equivalent) Data Test Set (Receiver) to the RCVR LINE jack on the front of the 3632–00. Refer to Figure 1 for the location of these jacks.
2.	Connect the data test set (transmitter and receiver) to the clock signal output jacks provided on the front panel of the LIU–3D or 3E by means of two Charles 93–369901 plug adaptors. (Insert the red plug of the adaptor cord into the BYTE jack and the blue plug into the BIT jack.)
3.	Perform both a subscriber's-end test and a far-end test of the facility according to the instructions provided in the manuals covering these data test sets.

9.   TECHNICAL ASSISTANCE

If technical assistance is required, contact Charles Industries' Technical Services Center at:

      847–806–8500
      847–806–8556 (FAX)
      800–607–8500
      techserv@charlesindustries.com (e-mail)

10.   WARRANTY & CUSTOMER SERVICE

10.1   Warranty

Charles Industries, Ltd. offers an industry-leading, 5-year warranty on products manufactured by Charles Industries. Contact your local Sales Representative at the address or telephone numbers below for warranty details. The warranty provisions are subject to change without notice. The terms and conditions applicable to any specific sale of product shall be defined in the resulting sales contract.

> Charles Industries, Ltd.
>
> 5600 Apollo Drive
>
> Rolling Meadows, Illinois 60008–4049
>
> 847–806–6300 (Main Office)
>
> 847–806–6231 (FAX)

10.2   Field Repairs (In-Warranty Units)

Field repairs involving the replacement of components within a unit are not recommended and may void the warranty and compatibility with any applicable regulatory or agency requirements. If a unit needs repair, contact Charles Industries, Ltd. for replacement or repair instructions, or follow the *Repair Service Procedure* below.

10.3   Advanced Replacement Service (In-Warranty Units)

Charles Industries, Ltd. offers an "advanced replacement" service if a replacement unit is required as soon as possible. With this service, the unit will be shipped in the fastest manner consistent with the urgency of the situation. In most cases, there are no charges for in-warranty repairs, except for the transportation charges of the unit and for a testing and handling charge for units returned with no trouble found. Upon receipt of the advanced replacement unit, return the out-of-service unit in the carton in which the replacement was shipped, using the pre-addressed shipping label provided. Call your customer service representative at the telephone number above for more details.

10.4   Standard Repair and Replacement Service (Both In-Warranty and Out-Of-Warranty Units)

Charles Industries, Ltd. offers a standard repair or exchange service for units either in- or out-of-warranty. With this service, units may be shipped to Charles Industries for either repair and quality testing or exchanged for a replacement unit, as determined by Charles Industries. Follow the *Repair Service Procedure* below to return units and to secure a repair or replacement. A handling charge applies for equipment returned with no trouble found. To obtain more details of this service and a schedule of prices, contact the CI Service Center at 217–932–5288 (FAX 217–932–2943).

Repair Service Procedure

1.   Prepare, complete, and enclose a purchase order in the box with the equipment to be returned.

2.   Include the following information:

   – Company name and address
   – Contact name and phone number
   – Inventory of equipment being shipped
   – Particulars as to the nature of the failure
   – Return shipping address

3.   Ship the equipment, purchase order, and above-listed information, transportation prepaid, to the service center address shown below.

   CI Service Center
   503 N.E. 15th St., P.O. Box 339
   Casey, IL 62420–2054

4.   Most repaired or replaced units will be returned within 30 or 45 days, depending on the product type and availability of repair parts. Repaired units are warranted for either 90 days from the date of repair or for the remaining unexpired portion of the original warranty, whichever is longer.

11.   SPECIFICATIONS

The electrical characteristics of the 3632–00 DS–0 DP channel unit are as follows:

11.1   Electrical

(a) INPUT/OUTPUT DATA RATE: 64KB/s DS–0 level.

(b) INPUT/OUTPUT SIGNAL FORMAT: Bipolar non-return-to-zero at DS–0 interface.

(c) INPUT/OUTPUT IMPEDANCE: 135 ohms $\pm$10 percent, balanced, DC-isolated at DS–0 interface.

(d) INPUT TRANSITION TIME: 5 microseconds maximum.

(e) INPUT VOLTAGE LEVEL RANGE: 1.5Vpk to 4.8Vpk.

(f) OUTPUT VOLTAGE LEVEL: 3.0V to 5.5Vpk when terminated in a 135 ohm $\pm$5 percent load resistance.

(g) OUTPUT TRANSITION TIME: 0.50 microseconds maximum.

(h) OUTPUT DRIVE CAPABILITY: Up to 1500 feet of 22 AWG balanced, twisted, shielded cable.

11.2   Physical

See Table 3 for the physical characteristics of the 3632–00.

Table 3. Physical Specifications

Feature	U.S.	Metric
Height	4.3 inches	10.9 centimeters
Width	1.36 inches	3.5 centimeters
Depth	10.4 inches	26.4 centimeters
Weight	8 ounces	227 grams
Temperature	32 to 122°F	0 to 50°C